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Indian Standard
METHODS OF MEASUREMENT OF ELECTRICAL CHARACTERISTICS OF MICROCIRCUITS

PART I DIGITAL MICROCIRCUITS

UDC 621·3·049·77 : 621·317·3

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Indian Standard
METHODS OF MEASUREMENT OF ELECTRICAL CHARACTERISTICS OF MICROCIRCUITS
PART I DIGITAL MICROCIRCUITS

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Indian Standard

METHODS OF MEASUREMENT OF ELECTRICAL CHARACTERISTICS OF MICROCIRCUITS

PART I DIGITAL MCROCIRCUITS

0. FOREWORD

0.1 This Indian Standard (Part I) was adopted by the Indian Standards Institution on 11 April 1980, after the draft finalized by the Semiconductor Devices and Integrated Circuits Sectional Committee had been approved by the Electronics and Telecommunication Division Council.

0.2 This standard, dealing with the methods of test for microcircuits has been prepared in two parts. The first part deals with digital microcircuits and the second part deals with analogue microcircuits.

0.3 The measurements and conditions are so specified as to achieve the required degree of accuracy. Additional test methods such as pulse methods have also been given which will give compatible results. By ' compatible ', it is meant that the value of the characteristic will fall within specified limits as for other methods when measured under specified condition.

0.4 While preparing this standard, assistance has been derived from the following:

IEC Pub 147-2 Essential ratings and characteristics of semiconductor device and general principles of measuring methods. International Electrotechnical Commission (IEC).

JSS 51400 (Part II) Test methods for microcircuits. Ministry of Defence, Government of India.

BS 9400-1970 Integrated Electronic Circuits of assessed quality : Generic data and methods of tests. British Standards Institution, UK.

0.5 In reporting the results of a test made in accordance with this standard, if the final value, observed or calculated, is to be rounded off, it shall be done in accordance with IS : 2-1960*.

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*Rules for rounding off numerical values (*revised*).

1. SCOPE

1.1 This standard (Part I) describes the methods of measurements of electrical characteristics for testing of digital microcircuits.

2. TERMINOLOGY AND LETTER SYMBOLS

2.1 Terminology — For the purpose of this standard, the terms and definitions given in IS : 1885 (Part VII/Sec 5)-1971* shall apply.

2.2 Letter Symbols — For letter symbols reference may be made to IS : 3715†.

3. GENERAL CONDITIONS

3.1 Unless otherwise stated, all tests shall be made under standard atmospheric conditions as specified in **3.1** of IS : 6553-1971‡. Before the measurements are made, the microcircuit shall be stored at the measuring temperature for a time sufficient to allow the entire circuit to reach this temperature. The recovery period specified shall also be sufficient for this purpose. When measurements are made at a temperature other than that specified, the ambient temperature during the measurement shall be recorded and the results shall be corrected, where necessary, to the specified temperature.

During measurements, the microcircuits shall not be exposed to draughts or direct sun-rays, and shall be protected from radioactive and electromagnetic radiations.

3.2 Electrical Test Conditions

3.2.1 *Ratings* — The test conditions for all measurements should be such that the maximum ratings of the device are not exceeded.

The precautions should include limits on maximum instantaneous currents and applied voltages. Devices should not be inserted into, nor removed from, a test circuit while the latter is energized.

3.2.2 *Equilibrium Conditions* — All electrical tests shall be conducted under equilibrium conditions unless otherwise specified or unless the measurement is being carried out under pulsed conditions. When test conditions cause significant change with time of the characteristic being measured, means of compensation for such effects will be specified; for example, the time duration that the device shall be maintained at test conditions before making a measurement.

---

*Electrotechnical vocabulary: Part VII Semiconductor devices, Section 5 Integrated circuits and microelectronics.

†Letter symbols for semiconductor devices (being issued in parts).

‡Environmental requirements for semiconductor devices and integrated circuits,

3.2.3 *Temperature*

3.2.3.1 Unless otherwise specified, all electrical measurements shall be made at an ambient or reference point temperature of 25 ± 3°C. Measurements may be carried out at temperatures other than 25°C provided that the device will be in accordance with all the provisions of the detail specification when tested at 25°C.

3.2.3.2 The ambient temperature shall be measured as the air temperature below the microcircuit in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

3.2.3.3 The reference point temperature for case rated microcircuits intended for conduction cooling through a mounting base shall be measured in accordance with the method given in Appendix A.

3.2.3.4 For circuits specified to be used under conditions other than ambient or conduction cooling, the temperature shall be measured as required by the detail specification.

3.2.4 *Measurement Circuit Requirements and Precautions*

3.2.4.1 *Open circuit* — A circuit shall be considered open-circuited if a two-to-one decrease in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of measurement. The values of high resistances (whether of circuit components or meters) specified in the circuits, would be so high that a two-to-one decrease in their value will not effect the desired accuracy of the measurement.

3.2.4.2 *Short circuit* — A circuit shall be considered short-circuited if a two-to-one increase in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. Capacitors used to couple or by-pass the test signal should present effective short circuits at the test frequency. In certain of the high frequency measurements, where RF decoupling is important, the necessary components and/or mounting conditions of the device shall be as specified.

3.2.4.3 *Small signal* — A signal shall be considered small if a two-to-one change in its magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. Care should be taken that the measuring equipment does not introduce spurious oscillation or distortion likely to affect the required accuracy of measurement.

3.2.4.4 *Constant current source* — A current source shall be considered constant if a two-to-one increase of a load impedance (*see* Note) does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.

3.2.4.5 *Current measuring device* — The effective admittance of a current measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of the test.

3.2.4.6 *Constant voltage source* — A voltage source shall be considered constant if a two-to-one decrease of a load impedance (*see* Note) does not produce a change in the parameter being measured that is greater than the required accuracy of measurement.

3.2.4.7 *Voltage measuring device* — The effective impedance of a valtage measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of measurement.

NOTE — A load in the conditions in **3.2.4.4** and **3.2.4.6** is chosen to represent the equivalent resistance of the test circuit and unit under test. For acceptance test purposes, the resistor value should represent the limiting conditions.

3.2.5 *Power Supplies* — The sources of direct currents and voltages should not have ripple contents large enough to affect the desired accuracy of measurement. Test or supply voltages or currents shall be within ± 1 percent of the specified value.

3.2.6 *Accuracy of Measurement* — The limits quoted in detail specification are absolute. Tolerance on measurements shall be taken into account when determining the actual measurement limits.

3.2.7 *Multiple Input/Output Devices* — Each functionally independent section of a multiple input/output devices shall be tested individually and all terminals associated solely with sections not under test shall be left open-circuited, or as specified.

Each of a group of functionally equivalent signal terminals shall be tested individually, with connections as specified in the detail specification applied to the remainder.

3.2.8 *Unspecified Connections to Terminals* — Any terminal for which no conditions are specified shall be left open-circuited.

4. VERIFICATION OF THE TYPE OF MICROCIRCUITS

4.1 Purpose — To confirm that the behaviour of microcircuit is in accordance with the concise description given in the detail specification. The method permits economic testing, with a high degree of assurance, to confirm that system operation will be attained. It is intended to be applied to all forms of microcircuits.

4.2 The circuit as shown in Fig. 1 shall be used.

4.3 Description — All inputs (signal and control) shall be operated in accordance with the intended function of the microcircuit and all resulting

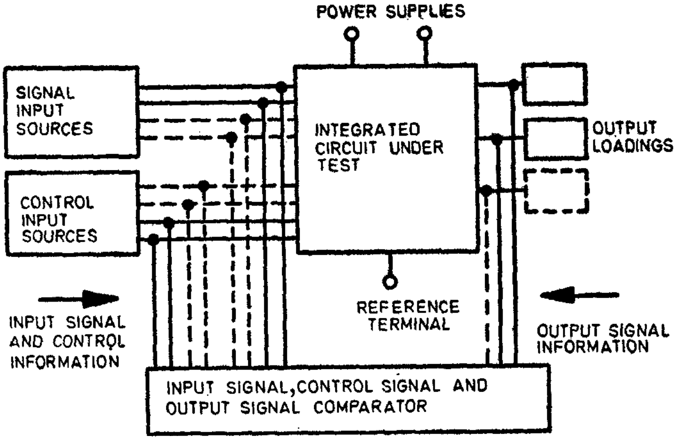

POWER SUPPLIES
SIGNAL INPUT SOURCES
CONTROL INPUT SOURCES
INTEGRATED CIRCUIT UNDER TEST
OUTPUT LOADINGS
REFERENCE TERMINAL
INPUT SIGNAL AND CONTROL INFORMATION
OUTPUT SIGNAL INFORMATION
INPUT SIGNAL, CONTROL SIGNAL AND OUTPUT SIGNAL COMPARATOR

FIG. 1 CIRCUIT FOR VERIFICATION OF THE TYPE OF MICROCIRCUIT

outputs shall be in accordance with that function. Digital circuits shall be tested in accordance with the specified function table at nominal supply voltages and with the input, control and output terminal voltages equal to the specified V_{OLA} and V_{OHB} values.

Terminals which are described as having no connections shall be so verified.

4.4 Procedure — The temperature conditions shall be 25°C nominal. The microcircuit is inserted into the test socket in accordance with its type designation marking and its terminal identification. These markings shall be legible and shall comply with the requirements of the detail specification. The supply voltages, input and control signals shall be set to their specified values and where necessary checked over their ranges and combinations and the outputs shall be verified for conformance to the requirement of the detail specification. The voltages and currents shall be reduced to zero and the microcircuit removed from the test socket.

4.5 Information to be Given in the Relevant Detail Specification

a) Supply voltages.

b) The input, control and output conditions and their interrelationship both coincidentally and sequentially.

5. MEASUREMENT OF STATIC CHARACTERISTIC OF DIGITAL CIRCUITS

5.1 It is necessary to test or measure the voltages for each state of output and to guarantee that these will be within specified limits when specified voltages are applied to the input terminals and when specified output currents are drawn from, or forced into, the output terminals.

5.1.1 The output voltages will lie within the ranges:

a) V_{OHA} and V_{OHB}, and

b) V_{OLA} and V_{OLB}.

Usually V_{OHA} cannot go higher than the positive supply voltage V_{CC}, and V_{OLB} can not go lower than the reference terminal voltage (generally zero).

5.1.2 The permitted ranges of the input voltages, set by the manufacturer, are:

a) V_{IHA} and V_{IHB}, and

b) V_{ILA} and V_{ILB}.

Usually V_{IHA} may not go higher than the positive supply voltage V_{CC}, and V_{ILB} may not go lower than the reference terminal voltage.

5.1.3 The currents associated with the input voltages represent the input consumption of each device and it is necessary to test or measure that the input consumption over the permitted range of input voltage is not outside specified or guaranteed limits. Also the currents associated with the output voltages represent the output capability of each device. The output capability is a design feature and is set by the manufacturer.

5.2 In the following test methods the permitted input voltages and the output currents are used as test conditions for the measurement of the output voltages. Thus V_{ILA} and I_{OHA} are used for the measurement of V_{OHE} for inverting gates and V_{IHB} and I_{OHA} are used for the measurement of V_{OHB} for non-inverting gates. Three of the static characteristics are effectively assessed by each measurement. Also the permitted input voltages are used for the measurement of the associated input currents.

5.3 Integrated circuits are designed to operate over a specified range of supply voltages and over a specified range of temperatures. The values of input and output voltages and currents will vary depending upon the supply voltage, the operating temperature and the input and output loadings.

5.4 For acceptance purposes it is not necessary to test and measure all the possible variations of the static characteristics. There are certain worst case conditions which give an overall limiting set of static characteristics and these have been chosen in the following test methods for this purpose. When used under conditions less onerous than the worst case conditions, for example, nominal supply voltages and 25°C ambient temperature, the values of the static characteristic will surpass those of the associated limits.

6. BREAKDOWN VOLTAGE

6.1 Purpose — This method establishes the means for assuring performance to the limits specified in the relevant detail specification in regard to input and output breakdown voltage.

6.2 Circuit — The circuit as shown in Fig. 2 shall be used.

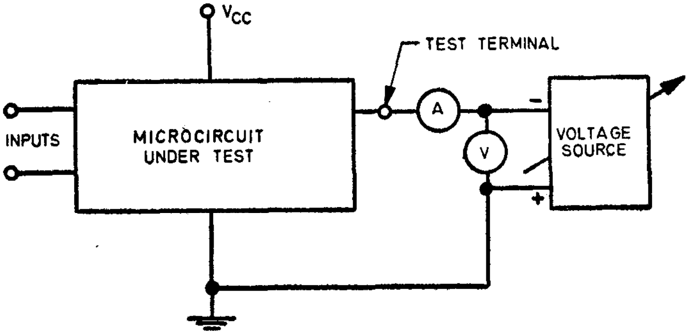


FIG. 2 CIRCUIT FOR THE MEASUREMENT OF BREAKDOWN VOLTAGE

6.3 Description — The test apparatus shall be capable of supplying the specified rated input or output voltage at the specified terminal and measuring the resultant terminal current. The test apparatus shall also be capable of applying the specified voltage and/or current levels to all other terminals. Care should be taken that the maximum device ratings are not exceeded during this test. The test chamber shall be capable of maintaining the device under test at any specified temperature.

6.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The microcircuit is inserted, in accordance with its marking, into the test socket. Except for the test terminal, all other terminals shall be conditioned as specified. The voltage on the test terminal shall be increased until either:

a) the specified maximum voltage is reached before the maximum current is reached, in which case the rating is proved; or

b) the specified maximum current is reached before the specific maximum voltage is reached, in which case the rating is not proved and the circuit is rejected.

Each input or output of multiple input or output devices shall be tested individually.

6.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage,

- b) Test terminal current,
- c) Signals, voltages or currents on other terminals, and
- d) Test temperature.

7. LOW-STATE INPUT CURRENT, I_{IL}

7.1 Purpose — To measure the low-state input current of a combination circuit under specified conditions.

7.2 Circuit — The circuit as shown in Fig. 3 shall be used.

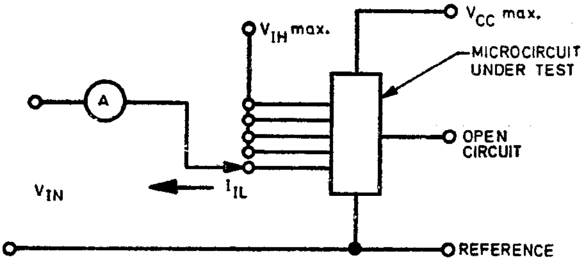


FIG. 3 CIRCUIT FOR THE MEASUREMENT OF LOW-STATE INPUT CURRENT

7.3 Description — The measurement shall be made under maximum specified supply voltage conditions. The output shall be open-circuit unless otherwise specified. The specified recommended maximum value of V_{OL} shall be applied to each input in turn. The other inputs shall be connected in parallel and taken to the specified value V_{IH} *max.* Sections of multiple gate circuits not being tested shall be left open-circuit or as specified.

7.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The microcircuit is inserted into the circuit in accordance with its marking. The supply voltage and input voltage are set to their specified values and the low-state input current measured. The voltages and currents are reduced to zero and the microcircuit removed from the test socket.

7.5 Information to be Given in the Relevant Detail Specification

- a) Supply voltage,
- b) Input voltage, and
- c) Ambient temperature.

8. HIGH-STATE INPUT CURRENT

8.1 Purpose — To measure the high-state input current of digital microcircuit under specified conditions.

8.2 Circuit — The circuit as shown in Fig. 4 shall be used.

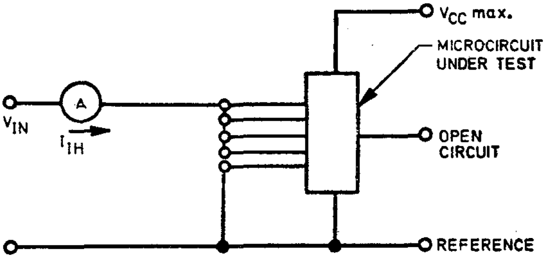


FIG. 4 CIRCUIT FOR THE MEASUREMENT OF HIGH-STATE INPUT CURRENT

8.3 Description — The test chamber shall be capable of maintaining the device under test at any specified temperature. The measurement shall be made under maximum recommended supply voltage conditions. The output shall be open-circuited unless otherwise specified. The specified value of input voltage shall be applied to each input in turn.

The other inputs shall be connected in parallel and taken to the reference voltage, usually zero.

8.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The microcircuit is inserted into the circuit in accordance with its marking. The supply voltage and input voltage are set to their specified values and the high-state input current measured. The voltages and currents are reduced to zero and the microcircuit removed from the test socket.

8.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage,
b) Input voltage, and
c) Ambient temperature.

9. LOW-STATE OUTPUT VOLTAGE (V_{OL})

9.1 Purpose — To measure the low-state output voltage of a digital microcircuit under specified input voltage, output loading and power supply conditions.

9.2 Circuit — The circuit as shown in Fig. 5 shall be used.

9.3 Description — The test instrument shall be capable of loading the output of the circuit under test with the specified positive or negative currents. Resistors may be used to simulate the specified current levels. The test

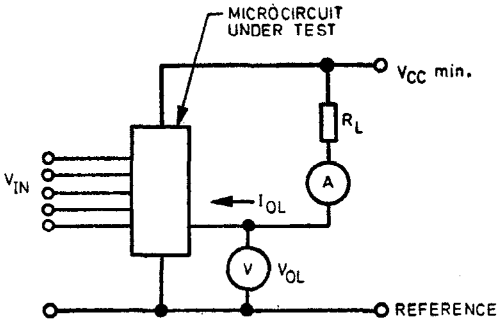


FIG. 5 CIRCUIT FOR THE MEASUREMENT OF LOW-STATE OUTPUT VOLTAGE

instrument shall be capable of supplying the worst case power supply and input voltages. The test chamber shall be capable of maintaining the device under test at any specified temperature. The measurement shall be made under the minimum specified supply voltage conditions. Resistor R_L is a load resistor adjusted to allow the maximum specified low-state output current to flow into or out of the output terminal or a current generator may be used. For TTL and DTL positive NAND gate circuits the minimum specified value of the high-state input voltage, V_{IHB} shall be connected to all input terminals in parallel. For TTL and DTL positive NOR gate circuits the minimum specified value of high-state input voltage V_{IHB} shall be connected to each input in turn, the other inputs being connected to the reference voltage usually zero. For TTL and DTL positive AND gate circuits the maximum specified value of the low-state input voltage V_{ILA} shall be connected to each input in turn, the other inputs being connected V_{IHB} or as specified. For TTL and DTL multiple gate circuits the appropriate input conditions to give the required low-state output voltage shall be used. Sections of multiple gates not being tested shall be left open-circuit or as specified.

For TTL and DTL digital gate circuits having extender input node terminals additional tests shall be made:

a) either with their associated extender circuits connected to their input node terminals and with the appropriate conditions applied to the extender input terminals; or

b) with specified input conditions applied to the node terminals.

For TTL and DTL digital gate circuits having open-collector output circuits, the test shall be made as specified in the detail specification.

For circuits other than TTL and DTL the input and output conditions of voltage and/or currents shall be as specified.

9.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The microcircuit is inserted into the circuit in accordance with its marking and terminal identification.

The supply voltage, input voltage and output current are set to their specified values and the output voltage is measured.

The voltages and currents are reduced to zero and the microcircuit removed from the test sockets.

9.5 Information to be Given in Relevant Detail Specification

a) Supply voltage,
b) Input voltage,
c) Output current, and
d) Ambient temperature.

10. HIGH-STATE OUTPUT VOLTAGE (V_{OH})

10.1 Purpose — To measure the high-state output voltage of a digital microcircuit under specified input voltage, output loading and power supply conditions.

10.2 Circuit — The circuit as shown in Fig. 6 shall be used.

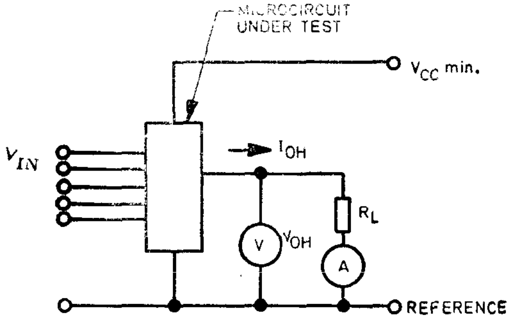


FIG. 6 CIRCUIT FOR THE MEASUREMENT OF HIGH-STATE OUTPUT VOLTAGE

10.3 Description — The test equipment shall be capable of loading the output of the circuit under test with the specified positive or negative currents. Resistors may be used to simulate the applicable current levels. The test equipment shall also be capable of supplying the worst case power supply and input voltages. The test chamber shall be capable of maintaining the device under test at any specified supply voltage conditions. Resistor R_L is a load resistor adjusted to allow the maximum specified high-state output current to flow into or out of the output terminal.

For TTL and DTL positive NAND gate circuits the maximum specified value of the low-state input voltage V_{ILA} shall be connected to all inputs in parallel.

For TTL and DTL positive NOR gate circuits the maximum specified value of the low-state input voltage V_{ILA} shall be connected to all inputs in parallel.

For TTL and DTL positive AND gate circuits the minimum specified value of high-state input voltage V_{IHB} shall be connected to all inputs in parallel.

For TTL and DTL positive OR gate circuits the minimum specified value of the high-state input voltage V_{IHB} shall be connected to each input in turn with the other inputs connected to the reference voltage, usually zero.

For TTL and DTL multiple gate circuits, the appropriate input condition to give the required high-state output voltage shall be used. Sections of multiple gates not being tested shall be left open-circuit or as specified.

For TTL and DTL digital gate circuits having extender input node terminals, additional tests shall be made:

a) either with their associated extender circuits connected to their input node terminals and with the appropriate conditions applied to the extender input terminals, or

b) with specified input conditions applied to the node terminals.

For TTL and DTL digital gate circuits having open-collector output circuits, the tests should be made as specified in the detail specification.

For circuits other than DTL and TTL the input and output conditions of voltage and/or currents shall be as specified.

10.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The microcircuit is inserted into the circuit in accordance with its marking and terminal identification.

The supply voltage, input voltage and output current are set to their specified values and the output voltage is measured.

The voltages and currents are reduced to zero and the microcircuit removed from the test socket.

10.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage,

b) Input voltage,

c) Output current, and

d) Ambient temperature.

11. OUTPUT VOLTAGES OF SEQUENTIAL BISTABLE MICROCIRCUITS

11.1 Purpose—To measure the high-state and low-state output voltages of sequential bistable circuits under specified conditions.

11.2 Circuit — The circuit as shown in Fig. 7 shall be used.

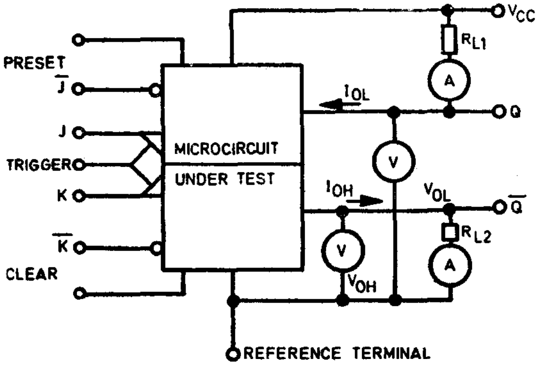


FIG. 7 CIRCUIT FOR MEASUREMENT OF OUTPUT VOLTAGE OF SEQUENTIAL BISTABLE

11.3 Description — The measurement shall be made under the minimum specified supply voltage conditions. The load resistors R_{L1} and R_{L2} shall be adjusted to allow the maximum specified low-state and high-state output currents to flow into or out of the output terminals; or current generators may be used. All steering inputs J and K, or R and S, as defined by the function table, shall be at V_{IHB} except as stated below:

All steering inputs J and K, or R and S, as defined by the function table shall be at the V_{ILA} except as stated below.

The trigger input shall be pulsed during each measurement with a rectangular waveform having the following characteristics:

Amplitude, not less than V_{OLA} to V_{OHB}

Duration, within the range 100 ns to 500 ns.

Rise and fall time, not greater than 15 ns.

a) V_{OL} at Q output and V_{OH} at $\overline{Q}$ output

The presetting (or direct set) input is put into the non-operative condition, zero volts or V_{CC} *min*.

The presetting cycle is — the clear (or direct reset) input is made operative and then non-operative.

b) V_{OL} at $\bar{Q}$ output and V_{OH} at Q output

The clear (or direct reset) input is put into non-operative condition, zero volts or V_{CC} *min*.

The presetting cycle is — the preset (or direct set) input is made operative and then non-operative.

In cases where clear (or direct reset) and/or preset (or direct set) terminals are not provided by the specified device, the circuit shall be set and cleared for test purposes either (a) by the application of signals to the appropriate input terminals in conjunction with trigger pulses according to the function table, or (b) by preconditoning at the outputs where this is appropriate.

11.4 Procedure — The temperature conditions shall be set to the specified value.

The microcircuit shall be inserted into the test socket in accordance with its marking and terminal identification. The supply voltages, input and control signals shall be set to their specified values in the prescribed sequence and the output voltages shall be measured.

The supply voltages and input and control signals shall be reduced to zero and the microcircuit removed from the test socket.

11.5 Information to be Given in the Relevant Detail Specification

a) Supply voltages;

b) The input, control and output conditions and their interrelationship, both coincidentally and sequentially; and

c) Ambient or case temperature.

12. INPUT CURRENTS FOR SEQUENTIAL BISTABLE CIRCUITS

12.1 Purpose — To measure the currents at each input terminal including control, for example, trigger, preset, clear, etc, terminals of sequential bistable circuits under specified conditions.

12.2 Circuit — The circuit as shown in Fig. 8 shall be used.

12.3 Description — The measurement shall be made under the maximum specified supply voltage conditions. Unless otherwise specified the measurements shall be made with the outputs open circuit.

For inputs in the low state, the current shall be measured with V_{OLA} connected to each input in turn with all other like inputs connected to V_{CC} *min*.

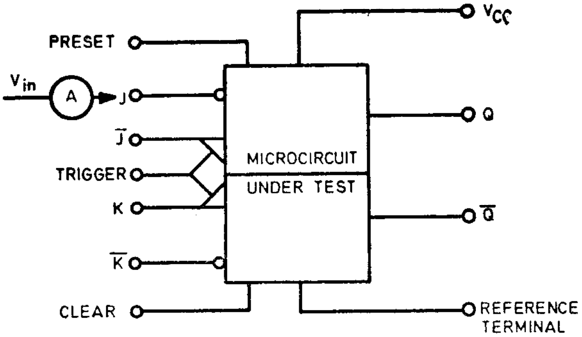


FIG. 8 CIRCUIT FOR THE MEASUREMENT OF INPUT CURRENTS FOR SEQUENTIAL BISTABLE CIRCUITS

For inputs in the high state, the current shall be measured with V_{OHB} connected to each input in turn with all other inputs connected to V_{CC} *min*.

Inputs associated with additional inverting gates shall be biased to give the appropriate state of the like inputs.

Where a presetting cycle is specified, the appropriate input shall be set to its operative condition, either V_{CC} *min* or zero volts, and then returned to its non-operative condition.

12.4 Procedure — The temperature conditions shall be set to the specified value.

The microcircuit shall be inserted into the test socket in accordance with its marking and terminal identification. The supply voltages, input and control signals shall be set to their specified values in the prescribed sequence and the input currents shall be measured.

The supply voltages and input and control signals shall be reduced to zero and the microcircuit removed from the test socket.

12.5 Information to be Given in the Relevant Detail Specification

a) Supply voltages;

b) The input and control conditions and their inter-relationship, both coincidentally and sequentially; and

c) Ambient or case temperature.

13. POWER SUPPLY CURRENT

13.1 Purpose — To measure the power supply current of microcircuits under specified conditions.

13.2 Circuit — The circuit as shown in Fig. 9 shall be used.

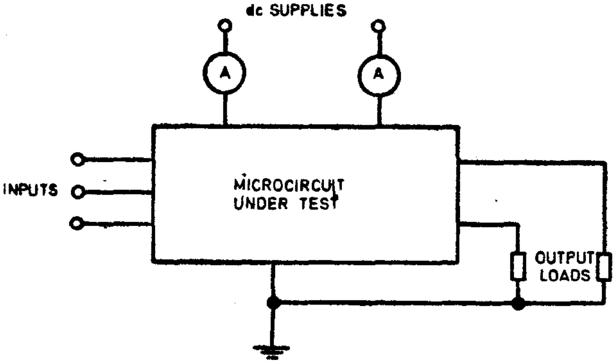


FIG. 9 CIRCUIT FOR THE MEASUREMENT OF POWER SUPPLY CURRENT

13.3 Description — The test apparatus shall be capable of supplying the necessary power, input signals, output loading and control signals as specified. The test chamber shall be capable of maintaining the device under test at any specified test temperature.

13.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement.

The microcircuit is inserted, in accordance with its marking, into the test socket. The supply voltages, input signals and control signals are increased to their specified values and the power supply currents (measured). The voltages, currents and signals are reduced to zero and the microcircuit removed from the test socket.

13.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage,
b) Input signals,
c) Control signals,
d) Output loadings (if applicable), and
e) Ambient or reference point temperature.

14. OUTPUT SHORT-CIRCUIT CURRENT

14.1 Purpose — To measure the output current of a microcircuit under specified conditions with the output short-circuited to the reference (ground) terminal.

14.2 Circuit — The circuit as shown in Fig. 10 shall be used.

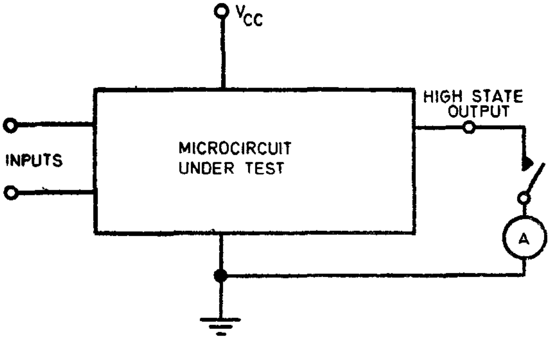


FIG. 10 CIRCUIT FOR THE MEASUREMENT OF OUTPUT SHORT CIRCUIT CURRENT

14.3 Description — The test chamber shall be capable of maintaining the device under test at any specified temperature.

The test apparatus shall be able to establish a short circuit at the output terminal after the particular output has been forced into the high state and to measure the resultant current flowing from the terminal.

14.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The microcircuit is inserted, in accordance with its marking, into the test socket. The supply voltage input and control signals are increased to their specified values in such a voltage on the specified output terminals shall be forced to zero and the resultant terminal current measured.

14.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage,

b) Input and control signals, and

c) Test temperature.

15. LOAD CONDITIONS

15.1 Purpose — To establish the load conditions to be used in measuring the dynamic performance of logic circuits such as DTL, RTL and ECL.

15.2 Description — The load for static tests shall simulate the worst case conditions for the circuit parameters being tested. The load for dynamic tests shall simulate a specified use condition for the parameters being tested. The loads shall be specified in the relevant specification.

15.3 Procedure

15.3.1 *Simulated Load* — The load shall simulate the specified conditions for the circuit parameters being tested. This load will represent the circuit parameters of the normal load as specified in the relevant detail specification.

15.3.2 *Discrete Component Load* — The load will consist of any combination of capacitive, inductive, resistive or diode components:

a) *Capacitive load* (C_L) — The specified load capacitance that the circuit under test may tolerate and still meet the dynamic performance specified shall be used. This will represent the input capacitance of the normal load for the device, the maximum line capacitance, and the probe and test fixture capacitance. The fixed value of capacitance shall be specified in the relevant detail specification.

b) *Inductive load* (L_L) — The specified load inductance that the circuit under test may tolerate and still meet the dynamic performance specified shall be used. This will represent the input capacitance of the normal load for the device, the maximum line capacitance, and the probe and text fixture inductance. The fixed value of inductance shall be specified in the relevant detail specification.

c) *Resistive load* (R_L) — The resistive load shall represent the specified fan-out conditions of the device under test. For sin loads, the resistor shall be connected between V_{CC} and gate output and for source loads, the resistor shall be connected between gate output and ground.

d) *Diode load* (D_L) — The diode load shall represent the input diode(s) of the circuit under test. The equivalent diode, as specified in the relevant detail specification, will also represent the base-emitter or base-collector diode of any transistor in the circuit path of the normal load.

15.3.3 *Dynamic Load Change* — The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular family of circuits being tested. One method of accomplishing this dynamic change is to use devices from the same logic family equal to the specified fan-out as the load.

NOTE — The load will normally be paralleled by a high impedance voltage detection indicator. The indicator may either be visual or memory storage.

15.4 Information to be Given in the Relevant Detail Specification

C_L, L_L, R_L, D_L and equivalent circuit.

16. NOISE MARGIN

16.1 Purpose — This method establishes the means of measuring the dc (steady state) and ac (transient) noise margin of digital microcircuits or to determine compliance with specified noise margin requirement in the relevant detail specification. It also provides assurance of interchangeability of devices and eliminates misunderstanding between manufacturers and users on noise margin test procedures and results. The standardization of particular combinations of test parameters (for example, pulse width, pulse amplitude, etc) does not preclude the characterization of devices under test with other variations in these parameters. However, such variations shall, where applicable, be provided as additional conditions of test and shall not serve as a substitute for the requirements established herein.

16.1.1 Noise margin levels are defined as follows:

a) *Low level noise margin*, V_{NL} — The low level noise margin or input voltage amplitude which may be algebracially added to V_{OLA} before the output level exceeds the allowed logic level (*see* Fig. 11).

b) *High level noise margin*, V_{NH} — The high level noise margin or input voltage amplitude which may be algebraically added to V_{OHB} before the output level exceeds the allowed logic level (*see* Fig. 11).

c) *Positive ground noise margin*, V_{NG+} — The positive voltage which may be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input levels.

d) *Negative ground noise margin*, V_{NG-} — The negative voltage which may be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input level.

e) *Power supply noise margin*, V_{NP+} — The positive voltage which may be algebraically added to the noise-free worst case most positive power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

f) *Power supply noise margin, negative*, V_{NP-} — The negative voltage which may be algebraically added to the noise-free worst case most negative (least positive) power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

16.1.2 Noise pulse width are defined as follows:

a) *Low level noise margin, pulse width*, t_{PL} — The low level noise pulse width, measured at the V_{ILA} level (*see* Fig. 11).

b) *High level noise margin, pulse width*, t_{PH} — The high level noise pulse width, measured at the V_{IHB} level (*see* Fig. 11).

16.1.3 The various noise levels shall be measured as shown in Fig. 11, 12 and 13.

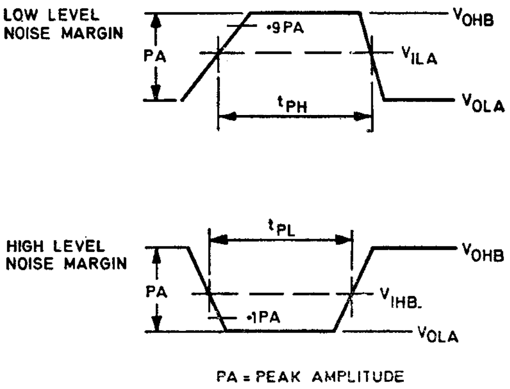


FIG. 11 DEFINITIONS OF NOISE PULSE WIDTH

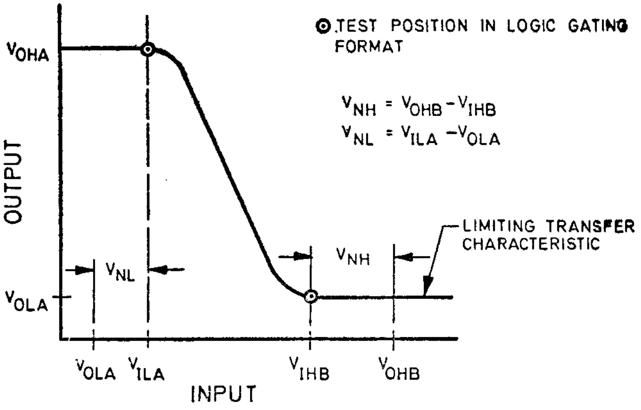


FIG. 12 INVERTING LOGIC GATE TRANSFER CHARACTERISTIC DEFINING TEST POINTS

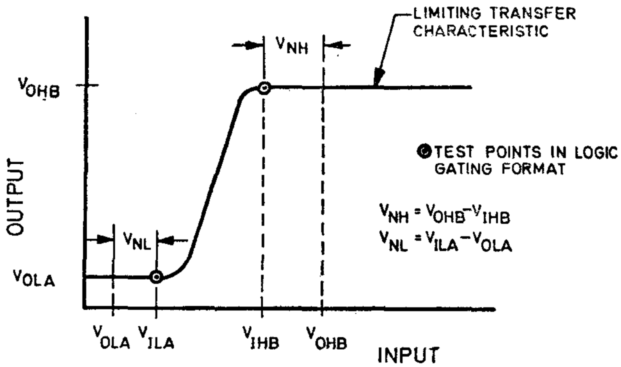


FIG. 13 NON-INVERTING LOGIC GATE TRANSFER CHARACTERISTIC DEFINING TEST POINTS

16.2 Description — Source generator, load and voltage detection devices for logic states, shall be used for noise margin measurement.

16.2.1 *Source Generator* — The source generator for this test shall be capable of supplying the required ac and dc noise inputs. In the case of pulsed inputs the transition times of the injected noise pulse shall each be maintained to less than 20 percent of the pulse width measured at the 50 percent amplitude level. For the purpose of this criteria, the transition times shall be between the 10 percent and 90 percent amplitude levels. The pulse repetition rate shall be sufficiently low that the element under test is at steady-state conditions prior to application of the noise pulse. For the purpose of this criteria, doubling the repetition rate or duty cycle shall not affect the outcome of the measurement.

16.2.2 *Load* — The load for this test shall simulate the circuit parameters of the normal load which would be applied in application of the device under worst-case conditions. The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular device load. The load shall be paralleled by a high impedance voltage detection device.

16.3 Procedure — The device shall be connected for operation using a source generator and load as specified above and measurements shall be made of V_{NL}, V_{NH}, V_{NP}, t_{PL} and t_{PH} following the procedures for both ac noise margin and dc noise margin (*see* Test procedure for dc and ac noise margin).

16.3.1 *General Consideration*

16.3.1.1 *Non-propagation of injected noise* — As defined, noise margin is the amplitude of extraneous signal which may be added to a noise-free worst case 'input' level before the output breaks the allowable logic levels.

This definition of noise margin allows the measurement of both dc and ac noise immunity on logic inputs or power supply lines or ground reference lines by detection of either a maximum low level or a minimum high level at the output terminal. Since the output level never exceeds the allowable logic level under conditions of injected noise, the noise is not considered to propagate through the element under test.

16.3.1.2 *Superposition of simultaneously injected noise* — Because the logic levels are restored after one stage, and because the noise margin measurement is performed with all 'inactive' inputs at the worst case logic levels, the proper system logic levels are guaranteed in the presence of simultaneous disturbances separated by at least one stage.

16.3.1.3 *Characterisation of ac noise margin* — Although the purpose of this standard test procedure is to insure interchangeability of elements by a single-point measurement of ac noise margin, the test procedure is well suited to the measurement of ac noise margin as a function of noise pulse width. In particular, for very wide pulse widths, the ac noise margin asymptotes to a value identically equal to the dc noise margin.

16.3.2 *Test Procedure for DC Noise Margin*

16.3.2.1 *Worst case configuration* — The measurement of dc noise margin using a particular logic input terminal should correspond to the worst case test configuration in the relevant detail specification. For example, the measurement of low level noise margin for a positive-logic inverting NAND gate should be performed under the same worst case test conditions as the dc measurement of V_{OHB}. If the worst case dc test conditions for V_{OHB} are high power supply voltage, all unused logic inputs connected to V_{OHB} and output current equal to zero, these conditions should be applied to the corresponding dc noise margin measurement.

16.3.2.2 *Low level noise margin,* V_{NL} — The low level noise margin test is normally performed during the V_{OH} test for inverting logic and during the V_{OL} test for non-inverting logic. The noise margin is calculated from the following expression:

$$V_{NL} = V_{ILB} - V_{OLA}$$

16.3.2.3 *High level noise margin,* V_{NH} — The high level noise margin test is performed during the V_{OL} test for inverting logic and during the V_{OH} test for non-inverting logic. The noise margin is calculated from the following expression:

$$V_{NH} = V_{OHB} - V_{IHB}$$

16.3.2.4 *Negative ground noise margin,* V_{NG} — With all power supply and output terminals connected to the appropriate worst case conditions, apply V_{OLA} to the inputs specified in the relevant detail specification and decrease the voltage applied to the ground terminal until the output levels equal V_{IHB} for inverting logic. The dc ground noise margin is the voltage measured at the device ground terminal. The dc source resistance of the injected ground line voltage shall be negligible.

16.3.2.5 *Positive ground noise margin,* V_{NG+} — With all power supply and output terminals connected to the appropriate worst case conditions, apply V_{OHB} to the input specified in the relevant detail specification and increase the voltage applied to the ground terminal until the output levels equal V_{ILA} for inverting logic and V_{IHB} for non-inverting logic. The dc ground noise margin is the voltage measured at the device ground terminal. The dc source resistance of the injected ground line voltage shall be negligible.

16.3.2.6 *Power supply noise margin,* V_{NP+} or V_{NP-} — With all input, power supply, and output terminals connected to the appropriate worst case conditions, increase (or decrease) the power supply voltage(s) until the output level equals the appropriate logic level limit. The power supply noise margin is the difference between the measured supply voltage(s) and the appropriate noise-free worst case supply voltage level(s). If more than one power supply is required, the noise margin of each supply should be measured separately.

16.3.3 *Test Procedure for AC Noise Margin*

16.3.3.1 *AC noise margin test point* — If, for any combination of noise pulse width or transition times, the ac noise margin is less than the dc noise margin, the noise pulse amplitude, pulse width, and transition time which produce the minimum noise margin shall be used as the conditions for test. If the ac noise margin exceeds the dc noise margin, the dc noise margin tests only shall be performed.

16.3.3.2 *Low level noise margin, pulse width,* t_{PL}—With all unused logic input, power supply, and output terminals connected to the appropriate worst case conditions, a positive-going noise pulse shall be applied to the input under test. The pulse amplitude shall be equal to V_{OHB} — V_{OLA}; the pulse shall be superimposed on a dc level equal to V_{OLA}; and the transition times shall be much less than the minimum transition times of the device under test. The test is performed by initially adjusting the input pulse width at the 0·9 amplitude level to one and one-quarter times the rise time. The pulse width is increased until the output voltage is equal to V_{IHA} for inverting logic and equal to V_{ILB} for non-inverting logic. The noise margin pulse width is then measured at the input pulse V_{ILA} level.

16.3.3.3 *High level noise margin, pulse width* t_{PH} — With all unused logic input, power supply, and output terminals connected to the appropriate worst case conditions, a negative-going noise pulse shall be applied to the input under test. The pulse amplitude shall be equal to V_{OHB} — V_{OLA}; the pulse shall be superimposed on a dc level equal to V_{OHB}; and the transition times shall be much less than the minimum transition times of the device under test. The test is performed by initially adjusting the input pulse width at the 0·1 amplitude level to one and one-quarter times the rise time. The pulse width is increased until the output voltage is equal to V_{ILB} for inverting logic measured at the input pulse V_{IHB} level.

16.4 Information to be Given in the Relevant Detail Specification

a) V_{ILA}
b) V_{ILB}
c) V_{IHB}
d) V_{IHA}
e) V_{OLA}
f) V_{OHB}
g) V_{NL}
h) V_{NG}
j) V_{NG}
k) V_{NP}
m) t_{PL}
n) t_{PH}
p) Test temperature. Unless otherwise specified dc noise margin measurements shall be made at the rate operating temperature extremes in addition to any other nominal test temperatures.
q) Specific noise margin measurements and conditions which are to be performed.
r) Power supply voltages.
s) Input conditioning voltages.
t) Output loads.
u) Parameters of noise signal.

17. LEAKAGE CURRENT

17.1 Purpose — To measure the leakage current at a terminal of a microcircuit.

17.2 Circuit — The circuits as shown in Fig. 14 shall be used.

17.3 Description — Resistor *R* should be of sufficient large value to protect the current meter *A* in the event of failure of the microcircuit being measured.

17.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The voltage source is set

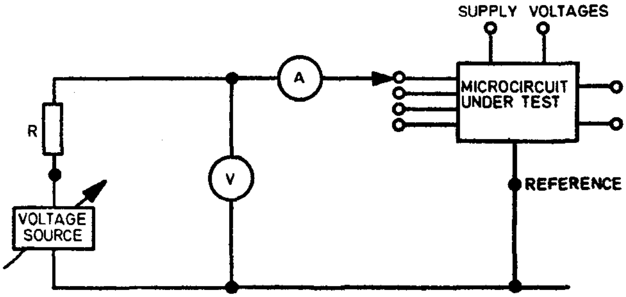


FIG. 14 CIRCUIT FOR THE MEASUREMENT OF LEAKAGE CURRENT

to a low value and the microcircuit is inserted into the test socket in accordance with its markings. The voltage is increased until the specified value is applied to the terminal under test, care being taken not to exceed the ratings during the adjustment. The leakage current is measured and the voltage is reduced to a low value. The test is repeated for each of the specified terminals and the microcircuit is removed from the test socket. Precautions should be taken to ensure that the leakage current due to the test circuit is insignificant.

17.5 Information to be Given in the Relevant Detail Specification

a) Test voltages,
b) Terminals to be tested,
c) Conditions at other terminals, and
d) Ambient or reference point temperature.

18. OUTPUT VOLTAGE FOR COMPLEX CIRCUITS

18.1 Purpose — To measure the high-state and low-state output voltages of complex circuits.

18.2 Circuit — The circuits as shown in Fig. 15 and 16 shall be used.

18.3 Description — The measurement shall be made under the minimum supply voltage conditions. The load resistances R_1 and R_2 shall be adjusted to allow the maximum specified low-state and high-state output currents to flow into and out of the output terminals; or current generators may be used in place of resistors. The sequences and combinations of input signals to give the appropriate output states shall be specified.

18.4 Procedure — The temperature conditions shall be set to the specified value. The microcircuit shall be inserted into the test socket in accordance

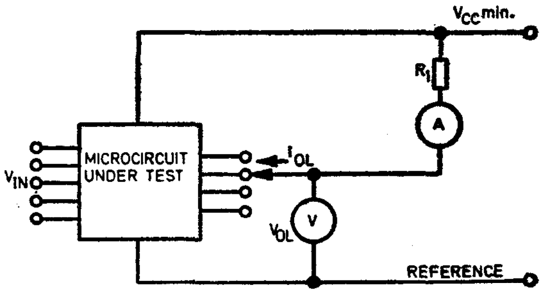


Fig. 15 Circuit for the Measurement of Low-State Output Voltages

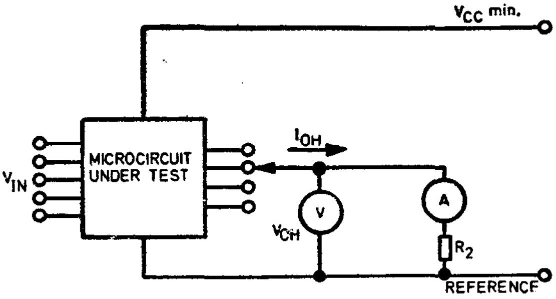


Fig. 16 Circuit for the Measurement of High-State Output Voltages

with its marking and terminal identification. The supply voltages, input and control signals shall be set to their specified values in the prescribed sequences and the output voltage(s) shall be measured. The output loading shall be as specified for the duration of the measurement.

18.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage;

b) The input, control and output conditions and their relationship, both coincidentally and sequentially; and

c) Ambient or reference point temperature.

19. TRANSIENT ENERGY RATING

19.1 Purpose — To determine the transient energy rating of an insulated gate microcircuit.

19.2 Circuit — The circuit as shown in Fig. 17 shall be used.

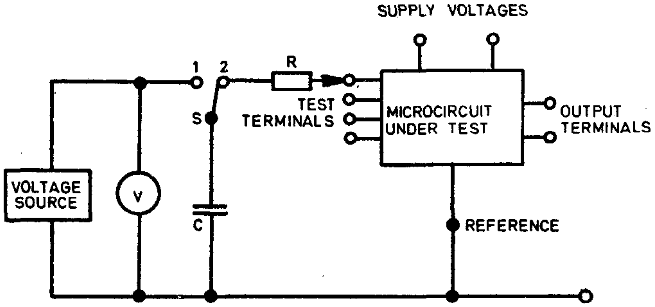


FIG. 17 CIRCUIT FOR THE MEASUREMENT OF TRANSIENT ENERGY RATING

19.3 Description — With switch *S* in position 1, capacitor *C* is charged to the specified test voltage. With the switch held in position 2, a discrete quantity of energy is available for presentation to the applicable terminal of the device under test. This cycle of operations is repeated for a specified number of times, after which the acceptability of the device is determined by post-test measurements. The voltage source shall be of low internal resistance compared with *R*. Switch *S* should be a mercury-wetted relay, or a switch having equivalent characteristics.

The following circuit values shall be used unless otherwise specified:

Test voltge	500 V
Capacitor *C*	100 pF
Resistor *R*	10 kΩ

19.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The microcircuit is inserted into the test socket. The voltage source is set to the specified value and the specified number of cycles of operation shall be applied in turn to each terminal except the reference terminal, other terminals being left unconnected. The microcircuit shall be removed from the test socket. The specified post-test measurements shall be made.

19.5 Information to be Given in the Relevant Detail Specification

a) Circuit values, if not as above: test voltage, capacitor *C* and resistor *R*;
b) Number of cycles of operation;
c) Post-test measurements;
d) Applicable terminal; and
e) Ambient or reference point temperature.

20. DRIVE SOURCE DYNAMIC

20.1 Purpose — To establish a drive source to be used in measuring dynamic performance of logic microcircuits.

20.2 Circuits — The circuits as shown in Fig. 18 and 19 shall be used.

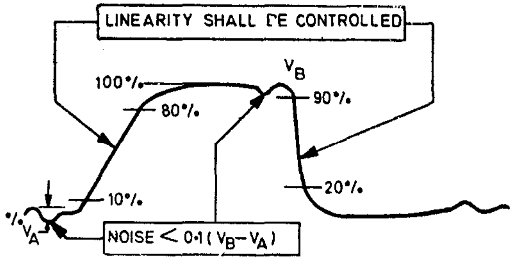


FIG. 18 DRIVE SIGNAL

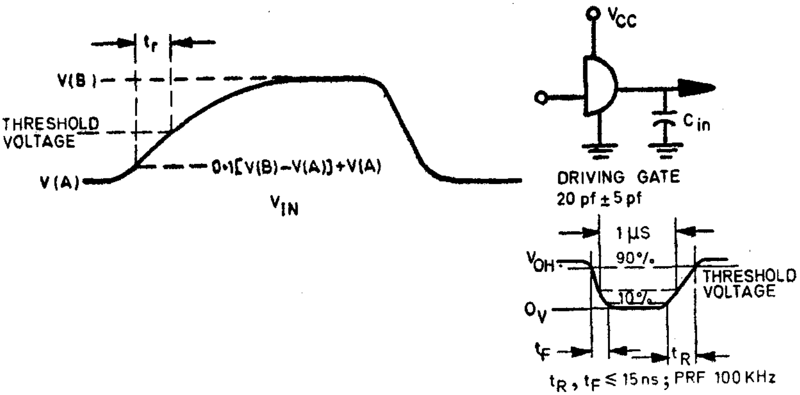


FIG. 19 DRIVE SOURCE (DYNAMIC)

20.3 Description

20.3.1 *TTL, DTL Circuits* — A driving source capable of supplying flat top and bottom signals with rise transitions that are linear from 10 percent to 90 percent and fall times that are linear from 90 percent to 20 percent shall be provided. The impedance of this driving source shall be sufficiently low to maintain signal levels and transition time linearities defined in the relevant detail specification. The driving signal is to be measured at the input terminal of the device under test with the device conditioned as specified. The driver source shall have controlled frequency, duty factor, signal levels and signal source shall have controlled frequency, duty factor, signal levels and signal transition times. Ringing and noise at both levels of the signal shall be controlled (0 to peak) to less than 10 percent of the total signal amplitude.

As an alternative driving source, a typical circuit, selected from the same family as the drive under test, shall be used as a driving source. This circuit, referred to as the driving gate, shall have an output rise time as specified. This rise time shall be defined $V_A + 0{\cdot}1\,(V_B - V_A)$ to the threshold voltage point and shall be measured with the device removed from the test circuit. The input to the driving gate shall be a source which has an up level of V_{OH} and a down level of 0 volts. In addition, it shall have the following characteristics:

t_r and $t_f \leqslant 15$ ns, and

PRF $\geqslant$ 100 kHz pulse width of negative portion + $1/n$ s at the threshold voltage point.

20.3.2 *ECL Circuits* — The driving source shall be considered the output of a bias driver of input gate driver. The bias driver shall be designed to assure that the threshold point of the circuit under test is always in the centre of the transition region as specified, and the input driver shall be selected from the same family as the device under test. The input to the driver shall be a source which has an up level of 0 volts and a down level of V_{OL}. In addition it shall have the following characteristics:

t_r and $t_f \leqslant 2$ ns, and

PRF $\geqslant$ 10 kHz, pulse width = 50 ns.

The input source of the driver should be terminated in its characteristic impedance Z_O at the test jig. Coaxial cables with the same Z_O should be used between the source and the driver. Ringing and noise at both levels of the signal shall be controlled (0 to peak) to less than 5 percent of the total amplitude.

20.3.3 *RTL Circuits* — Two typical circuits selected from the same family as the device under test or an appropriate driving circuit shall be used as the driving source. This circuit(s) shall have an output rise time as specified. This rise time shall be defined from $V_A + 0{\cdot}1\,(V_O - V_A)$ to $V_A + 0{\cdot}9\,(V_B - V_A)$ and shall be measured with the device under test removed from the test circuit. The input to the driving gate shall be a source which has an up level of V_{OH} and a down level of 0 volts. In addition, it shall have the following characteristics:

$t_r = 50$ ns,

PRF = 1 000 kHz pulse, width = 100 ns

20.4 Procedure

20.4.1 *TTL, DTL Circuits* — Using the driving source of TTL, DTL circuits described in **20.3.1**, the various parameters of driving signal shall be defined in the relevant detail specification. Level V_A shown in the circuit is critical to t_{PDL} delay and should be taken to adjust this level to within 20 mV of the specified level with a device under test in the test circuit. Level V_B shall be specified as a nominal V_{OH}. The driving signal shall be measured at the input termimal of the test circuit. The test circuit shall be switched by the driving signal and have normal bias voltages applied.

Using the alternate driving source of **20.3.1**, signal V_{IN} shown in the circuit shall be adjusted to the specified t_r in the detail specification with the device under test removed from the test circuit. t_r may be adjusted by selecting driving gate circuits or adjusting C_{IN}. Level V_A shall be specified as a nominal V_{OL}. Level V_B shall be specified as a nominal V_{OH}.

20.4.2 *ECL Circuits* — The output of the bias driver and input gate driver shall be adjusted to the specified t_r and threshold point in the relevant detail specification, with the device under test removed from the test circuit. For the bias driver, t_r may be adjusted by varying C_{IN} or adjusting the source driving the bias driver and the threshold point is adjusted by varying the bias driver voltage ($-V$).

20.4.3 *RTL Circuits* — The signal V_{IN} shown in the circuit shall be adjusted to the specified t_r in the relevant detail specification with the device under test removed from the test circuit. Level V_A shall be specified as a nominal V_{CL} and level V_B shall be specified as a nominal V_{OH}.

20.5 Information to be Given in the Relevant Detail Specification

a) Levels V_A and V_B, where applicable;
b) During signal transition times;
c) Repetition frequency and duty factors;
d) Driving gate and/or circuit, where applicable;
e) Bias driver, where applicable; and
f) C_{IN}, where applicable.

21. SWITCHING DELAY TIME AND TRANSITION TIMES

21.1 Purpose — To measure the delay time and transition time of digital integrated circuits when switched from one defined state to another under specified conditions.

21.2 Circuit — The circuit as shown in Fig. 20 shall be used.

21.3 Description — These measurements are intended to measure the delay and transition times for inverting and/or non-inverting digital circuits whose inputs and outputs are loaded with specified passive networks. The time constants and impedances of the driving and loading networks shall be established by means of linear passive components. The input and output

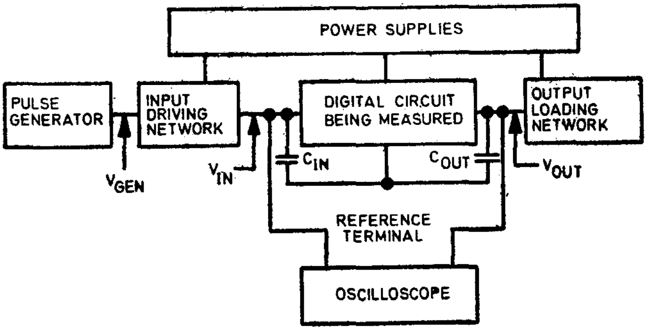


FIG. 20 CIRCUIT FOR THE MEASUREMENT OF SWITCHING DELAY TIME AND TRANSITION TIMES

capacitances C_{IN} and C_{OUT} shall be as specified and shall include all parasitic capacitances present in the driving and loading networks and any stray capacitances associated with the mounting jig and test fixtures, but exclude the parasitic capacitances presented by the microcircuit being measured. C_{IN} and C_{OUT} may be included in the input and output networks where appropriate. When required, the network configuration shall be as specified.

The values of the source impedance of the pulse generator and the characteristics of the pulse waveform shall be as specified.

The dc bias conditions, including the bias on all unused inputs and outputs of the microcircuits being measured, shall be as specified.

The delay and transition times are measured from the waveforms displayed on the oscilloscope reference Fig. 21. The input impedance of the oscilloscope should be high compared with the input and output impedances of the microcircuits being measured. If necessary an equivalent time measuring instrument may be used in place of the oscilloscope.

The amplitude of the input waveform shall not be less than that shown in Fig. 21. The upper and lower amplitude levels shall be set up with the input network driving a dummy load which is representative of the type of circuits being measured.

The reference levels from which the time intervals are measured are indicated in Fig. 21. They are chosen to lie midway between V_{CC} and V_{OHB}, V_{OHB} and V_{IHB}, V_{IHB} and V_{ILA}, V_{ILA} and V_{OLA} and V_{OLA} and zero. These reference levels are chosen so that protection is ensured against noise inputs up to 50 percent of the dc high state and/or 50 percent of the dc low state.

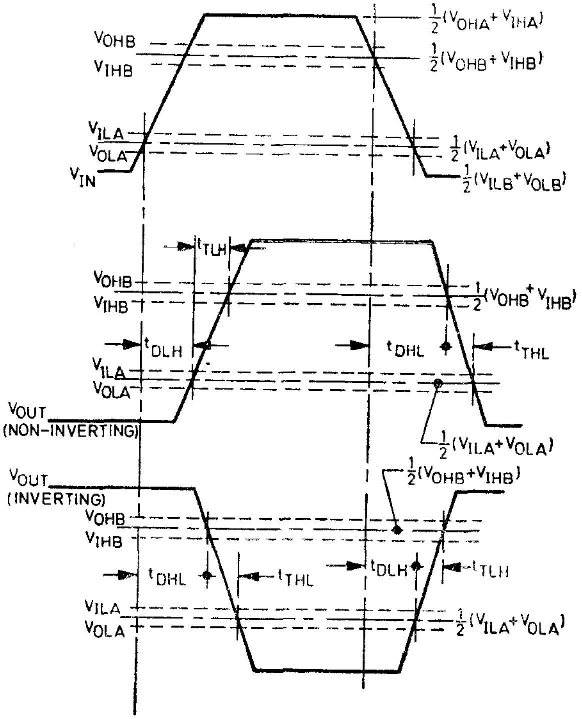

$\frac{1}{2}(V_{OHA}+V_{IHA})$
V_{OHB}
V_{IHB}
$\frac{1}{2}(V_{OHB}+V_{IHB})$
V_{ILA}
V_{OLA}
V_{IN}
$\frac{1}{2}(V_{ILA}+V_{OLA})$
$\frac{1}{2}(V_{ILB}+V_{OLB})$
t_{TLH}
V_{OHB}
V_{IHB}
$\frac{1}{2}(V_{OHB}+V_{IHB})$
t_{DLH}
t_{DHL}
t_{THL}
V_{ILA}
V_{OLA}
V_{OUT} (NON-INVERTING)
$\frac{1}{2}(V_{ILA}+V_{OLA})$
$\frac{1}{2}(V_{OHB}+V_{IHB})$
V_{OUT} (INVERTING)
V_{OHB}
V_{IHB}
t_{DHL}
t_{THL}
t_{DLH}
t_{TLH}
V_{ILA}
V_{OLA}
$\frac{1}{2}(V_{ILA}+V_{OLA})$

FIG. 21 INPUT AND OUTPUT WAVEFORMS WITH REFERENCE LEVELS FOR TIME INTERVAL MEASUREMENT

21.4 Procedure — The temperature conditions shall be set to the specified value. The integrated circuit shall be inserted into the test socket in accordance with its marking and terminal identification. The supply voltages and pulse generator signals shall be set to their specified values and the delay and transition times measured as follows:

t_{DHL} — the delay time with the output changing from the high to low state. In the case of inverting device it is measured between the input point defined as $\frac{1}{2}$ (V_{ILA} + V_{OLA}) and the output defined as $\frac{1}{2}$ (V_{OHB} + V_{IHB}). In the case of a non-inverting device, it is measured between the input and output points defined as $\frac{1}{2}$ (V_{OHB} + V_{IHB}).

t_{THL} — the transition time with the output changing from the high to low state, measured between the output point defined as $\frac{1}{2}$ (V_{OHB} + V_{IHB}) and the output point defined as $\frac{1}{2}$ (V_{ILA} + V_{OLA}).

t_{DLH} — the delay time with the output changing from the low to high state. In the case of the inverting device, it is measured between the input point defined as $\frac{1}{2}$ ($V_{OHB} + V_{IHB}$) and the output point defined as $\frac{1}{2}$ ($V_{ILA} + V_{OLA}$). In the case of a non-inverting device, it is measured between the points defined as $\frac{1}{2}$ ($V_{ILA} + V_{OLA}$).

t_{TLH} — the transition time with the output changing from the low to high state, measured between the output point defined as $\frac{1}{2}$ ($V_{ILA} + V_{OLA}$) and the output point defined as $\frac{1}{2}$ ($V_{OHB} + V_{IHB}$).

The supply voltages and input signals shall be reduced to zero and the integrated circuit removed from the test socket.

21.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage,

b) The amplitude and pulse characteristics of the input signal, and

c) The input and output network characteristics including C_{IN} and C_{OUT}.

22. SWITCHING PROPAGATION TIMES

22.1 Purpose — To measure the propagation times of digital integrated circuits when switched from one defined state to another under specified conditions.

22.2 Circuit — The circuit as shown in Fig. 22 shall be used.

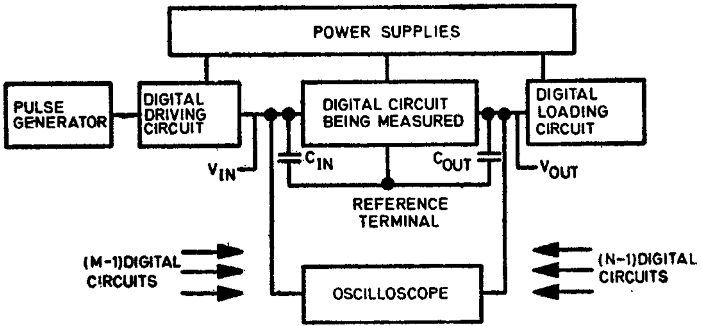


FIG. 22 CIRCUIT FOR THE MEASUREMENT OF SWITCHING PROPAGATION TIMES

22.3 Description — These methods are intended to measure the propagation times for inverting and/or non-inverting digital circuits whose inputs and outputs are loaded with specified digital circuits. The microcircuits which are used for the input driving and output loading circuits should have typical characteristics representative of the microcircuits intended to be normally connected to the microcircuit being measured. The number of circuits driven in parallel by both the driving circuit (M) and the microcircuit under test (N) should be as specified and should represent the worst case for each of the two times being measured. The typical characteristics for the input and output loading circuits should be chosen according to the results of measurements made using method given in **21**. The input and output capacitances C_{IN} and C_{OUT} shall be as specified and shall include all parasitic capacitances present in the driving and loading networks and any stray capacitances associated with the mounting jig and test fixtures, but exclude the parasitic capacitances presented by the microcircuit being measured. Care should be taken to avoid inductive effects in the connecting leads to the test mounting. When specified the driving and loading circuits may be replaced by equivalent specified networks.

The values of the impedance of the pulse sources and the characteristics of the pulse waveform shall be as specified.

For combinatorial circuits the dc bias conditions, including the bias on all unused inputs and outputs of the microcircuits being measured, shall be as specified. In addition for all other circuits the input combinations and sequences specified to give the required changes in an output state shall be derived from a set of pulse sources which are linked in frequency and phase relationships.

The input impedance of the oscilloscope should be high compared with the input and output impedances of the microcircuits being measured. If necessary an equivalent time measuring instrument may be used in place of the oscilloscope. Neither type of instrument should introduce a significant differential delay.

The amplitude of the input waveform shall be not less than in Fig. 23. The upper and lower amplitude levels shall be set up with the input network driving a dummy load which is representative of the type of circuit being measured.

The delay and transition times are measured from the waveforms displayed on the oscilloscope. The reference levels from which the time intervals are measured are indicated in Fig. 23. They are chosen to lie midway between the specified values of V_{IHB} and V_{ILA}.

22.4 Procedure — The temperature conditions shall be set to the specified value.

The microcircuit shall be inserted into the test socket in accordance with its marking and terminal identification. The supply voltages and pulse

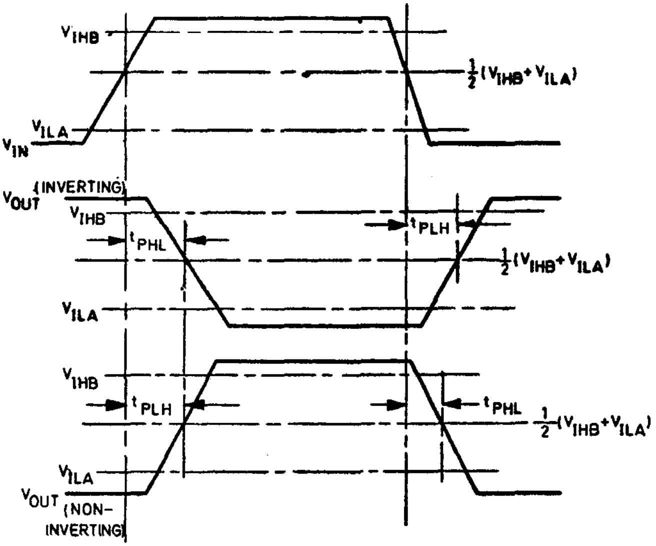


FIG. 23 INPUT AND OUTPUT WAVEFORMS WITH REFERENCE LEVELS FOR SWITCHING TIME MEASUREMENTS

source signals shall be set as specified and the propagation times measured as follows:

t_{PHL} — the time delay with the defined output changing from the defined high state to the defined low state, measured between points on the input and output waveforms defined as $\frac{1}{2}$ (V_{IHB} + V_{ILA}).

t_{PLH} — the time delay with the defined output changing from the defined low state to the defined high state, measured between points on the input and output waveforms defined as $\frac{1}{2}$ (V_{IHB} + V_{ILA}).

The supply voltages and input signals shall be reduced to zero and the integrated circuit removed from the test socket.

22.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage;
b) The input control and output conditions and their inter-relationship both coincidentally and sequentially;
c) The amplitude and pulse characteristics of the input signal;
d) The number of input and output circuit including C_{IN} and C_{OUT} or the equivalent input and output networks;
e) Ambient or reference point temperature.

23. BISTABLE SWITCHING TIMES (SET-UP TIME, HOLD TIME)

23.1 Purpose — To measure the set up time and hold time of the logic input relative to the trigger input of a bistable, necessary to produce correct switching.

23.2 Circuit — The circuit as shown in Fig. 24 shall be used.

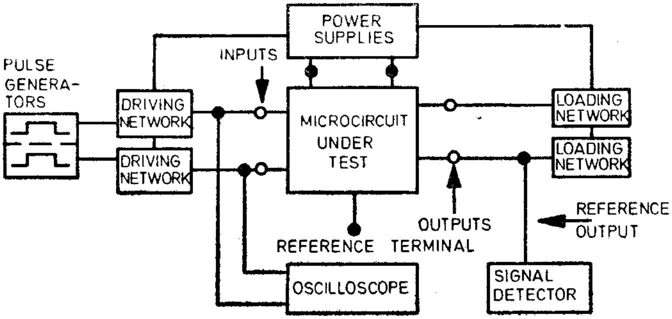


FIG. 24 CIRCUIT FOR THE MEASUREMENT OF BISTABLE SWITCHING TIMES

23.3 Description — A bistable will switch into its opposite state when the appropriate signal level applied to the logic input(s) coincides for a given time interval with a specified level and/or transition applied to the trigger input. Failure to switch occurs when the duration of coincidence is less than a value which is the characteristic for the microcircuit under test.

In Fig. 24 the pulse generator(s) shall provide two output pulses which are synchronized but adjustable in phase relative to each other. For certain classes of bistable (for example D-type) the delayed pulse shall have a repetition frequency half that of the reference pulse. This will be specified in the detail specification. Otherwise both pulses shall have the same repetition frequency.

Driving and loading networks shall be connected when and as specified.

Unused inputs, for example, direct set and clear, shall be connected to specified bias voltages, usually chosen from zero volts and V_{OHB}.

The input impedance of the oscilloscope and the signal detector shall be high compared with the impedances at the input and output measuring point. An equivalent time measuring instrument may be used in place of the oscilloscope. Neither type of instrument shall introduce a significant differential delay.

The signal detector may be an oscilloscope or any other instrument which may indicate whether or not the output of the bistable switches continuously between its two levels at half of the frequency of the triggering pulses.

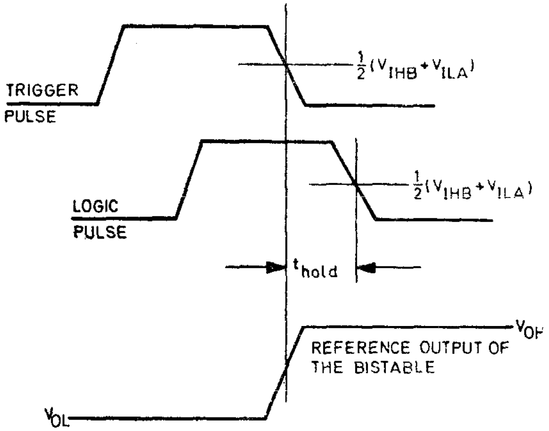
23.4 Procedure — The microcircuit is connected into the test circuit in accordance with its markings, and the supply and bias voltages set to within 1 percent of the specified values.

The temperature conditions are set to the specified value and checked before and after the measurement.

The pulse generator output pulses are increased to give the specified amplitude and their duration and repetition frequency(ies) set to the specified values.

The time delay, as measured between the points at $\frac{1}{2}$ ($V_{IHB} + V_{ILA}$) on the specified transitions of the logic pulse and the trigger pulse is increased from zero. The output level of the bistable is observed to note when the required change of level occurs. The corresponding time delay is measured.

The measurement will give either the set-up or hold time according to which pair of appropriate transitions is selected (*see* Fig. 25 and 26).


TRIGGER PULSE
$\frac{1}{2}(V_{IHB}+V_{ILA})$
LOGIC PULSE
$\frac{1}{2}(V_{IHB}+V_{ILA})$
t_{hold}
V_{OH}
REFERENCE OUTPUT OF THE BISTABLE
V_{OL}

NOTE 1 — The change of output level of the bistable is coincident with the negative-going edge of the trigger pulses.

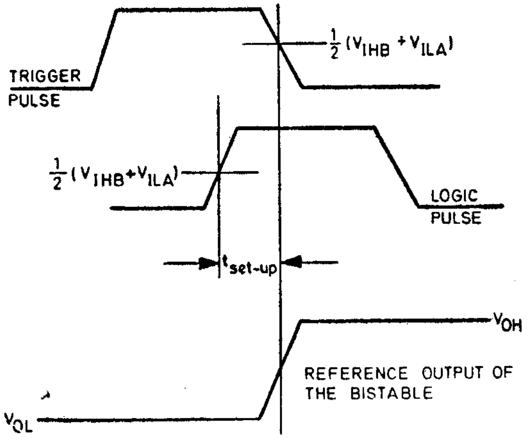
NOTE 2 — The waveform shown is of arbitrary polarity.

FIG. 25 TYPICAL WAVEFORMS INDICATING ' SET-UP TIME '

24. SWITCHING FREQUENCY OF A SEQUENTIAL CIRCUIT

24.1 Purpose — To determine whether the maximum (minimum) switching frequency of a sequential microcircuit lies above (below) a specified limit.

24.2 Circuit — The circuit as shown in Fig. 27 shall be used.


TRIGGER PULSE
$\frac{1}{2}(V_{IHB}+V_{ILA})$
$\frac{1}{2}(V_{IHB}+V_{ILA})$
LOGIC PULSE
$t_{set\text{-}up}$
V_{OH}
REFERENCE OUTPUT OF THE BISTABLE
V_{OL}

NOTE 1 — The change of output level of the bistable is coincident with the negative-going edge of the trigger pulse.

NOTE 2 — The wave-form shown is of arbitrary polarity.

FIG. 26 TYPICAL WAVEFORMS INDICATING ' HOLD TIME '

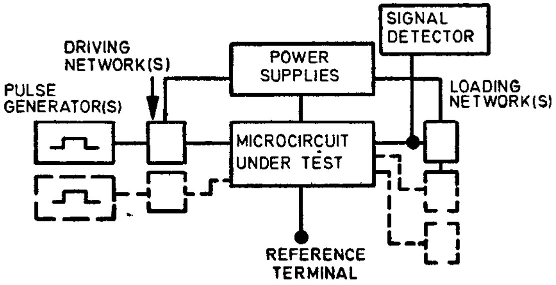


FIG. 27 CIRCUIT FOR THE MEASUREMENT OF SWITCHING FREQUENCY

24.3 Description — A sequential circuit, which may be in particular a bistable or a counter or a shift register, will switch into a different state when (a) the appropriate triggering stimulus has been absent for a given time, and then (b) the appropriate triggering stimulus is applied for a given time. These two periods of time need not be equal.

Failure to switch at maximum frequency will occur when the sum of these two times in any single cycle falls below a value which determines this characteristic at minimum frequency for the microcircuit.

For certain classes of sequential circuit, control signals may be required from additional pulse generators. The output pulses of the additional generators shall be synchronized with but adjustable in time delay relative to the first, and have a frequency which is an integral division of the first.

Loading networks for both tested and untested outputs, and driving networks shall be connected when and as specified.

Unused inputs shall be connected to specified bias voltages, usually chosen from zero voltage and V_{OHB} or else left unconnected.

The signal detector shall include an oscilloscope or other instruments which may indicate whether or not the tested output of the sequential circuit switches between its two states at a specified frequency, this being related to that of the triggering pulses. It shall also be able to indicate that the output signal satisfies the limits for V_{OHB} value of V_{OLA} value between each transition.

24.4 Procedure — The microcircuit is connected into the test circuit in accordance with its markings, and the supply and bias voltages set to within 1 percent of their specified values.

The temperature conditions are set to the specified value and checked immediately before and after the measurement.

The pulse generator output pulses are increased to give the specified amplitude. Their duration and repetition frequency are set to the specified values. Any other pulse generator required is similarly adjusted and the delay(s) between them set to the specified value(s).

The output of the microcircuit shall be observed, *via* the signal detector, for correct switching at the specified output frequency.

24.5 Information to be Given in the Relevant Detail Specification

a) Supply voltage(s);

b) Pulse generator characteristics: amplitude, duration, output impedance, rise and fall times, repetition frequency and, when appropriate, delay between pulses from differential generators;

c) Output loading network(s) for both tested and untested outputs:

d) Input driving network, if required;

e) Repetition frequency of output signal;

f) Conditions at unused terminals; and

g) Ambient temperature.

25. SMALL-SIGNAL CAPACITANCE

25.1 Purpose — To measure the small-signal capacitance at an input or output of a microcircuit under specified conditions.

25.2 Circuit — The circuit as shown in Fig. 28 shall be used.

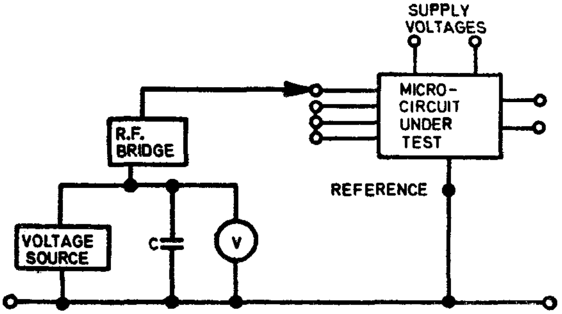


FIG. 28 CIRCUIT FOR MEASURING SMALL SIGNAL CAPACITANCE

25.3 Description — The RF bridge should have low internal dc resistance and should be capable of carrying the required reverse current of the input or output being measured without affecting the accuracy of measurement. Alternatively, other methods of biasing the circuit may be used. Small-signal conditions of measurement shall apply. Capacitor *C* shall present a short circuit at the test frequency which shall be 1 MHz unless otherwise specified. The equipment shall be capable of applying 1 MHz controllable amplitude signal superimposed on a variable plus or minus dc voltage.

25.4 Procedure — The temperature conditions are set to the specified value and checked before and after the measurement. The RF bridge is balanced without the microcircuit in the test socket but with the rest of the test circuit connected and with the reverse voltage set to the specified value. The microcircuit is inserted into the test socket, the reverse voltage is checked and the RF bridge is again balanced. The capacitance of the input or output is measured as the difference between the two readings of the bridge.

25.5 Information to be Given in the Relevant Detail Specification

a) Reverse voltage,
b) Conditions at other terminals,
c) Measurement frequency (if different from 1 MHz), and
d) Ambient or reference point temperature.

APPENDIX A

(*Clause* 3.2.3.3)

REFERENCE POINT TEMPERATURE

A-1. PURPOSE

A-1.1 To measure the reference point temperature, case or stud, of a conduction cooled integrated circuit under specified conditions.

A-2. DESCRIPTION

A-2.1 The temperature is measured by means of a thermocouple fitted into a high-conductivity copper spacer inserted between the integrated circuit and the heat sink.

The thermocouple wires should not be greater than 0·25 mm diameter.

A-2.2 The spacer shall be 3 mm thick, of approximately the same size and shape as the mounting base of the device. The disposition and sizes of the holes in the device, the copper spacer and the heat sink shall be the same.

A-2.3 The thermocouple shall be fixed into a 2 mm diameter hole drilled into the edge of the spacer to the centroid or to within 0·5 mm of the central hole as appropriate.

A-3. PRECAUTIONS

A-3.1 Care should be taken to ensure that the thermocouple is fully inserted into the hole of the spacer. Where a mica washer is used, it should be placed between the spacer and the heat sink.

A-4. PROCEDURE

A-4.1 The temperature is measured under specified conditions by means of the thermocouple.

A-5. SPECIFIED CONDITIONS

A-5.1 The following conditions will be obtained from the detail specification:

a) Test conditions;

b) Test equipment, if required.

INTERNATIONAL SYSTEM OF UNITS (SI UNITS)

Base Units

Quantity	*Unit*	*Symbol*
Length	metre	m
Mass	kilogram	kg
Time	second	s
Electric current	ampere	A
Thermodynamic temperature	kelvin	K
Luminous intensity	candela	cd
Amount of substance	mole	mol

Supplementary Units

Quantity	*Unit*	*Symbol*
Plane angle	radian	rad
Solid angle	steradian	sr

Derived Units

Quantity	*Unit*	*Symbol*	*Definition*
Force	newton	N	1 N = 1 kg. m/s^2
Energy	joule	J	1 J = 1 N.m
Power	watt	W	1 W = 1 J/s
Flux	weber	Wb	1 Wb = 1 V.s
Flux density	tesla	T	1 T = 1 Wb/m^2
Frequency	hertz	Hz	1 Hz = 1 c/s (s^{-1})
Electric conductance	siemens	S	1 S = 1 A/V
Electromotive force	volt	V	1 V = 1 W/A
Pressure, stress	pascal	Pa	1 Pa = 1 N/m^2